WHAT IS CLAIMED IS:

1. A method comprising:

calculating, in parallel, a first multiplication product of a first coefficient and a first sample, and a second multiplication product of the first coefficient and a second sample; and

wherein the first sample and the second sample are from a plurality of sequential samples;

wherein the first sample is an (n)th sample and the second sample is an (n+2)th sample in the plurality of sequential samples.

2. The method as recited in Claim 1, further comprising:

full scale negative testing the first sample and the second sample.

3. The method as recited in Claim 1, further comprising:

accumulating subsequent multiplication products with the first multiplication product into a final product.

4. The method as recited in Claim 3, further comprising:

saturating the final product.

5. The method as recited in Claim 1, wherein the first sample and second sample are odd samples in the plurality of sequential samples.

6. The method as recited in Claim 1, wherein the first sample and second sample are even samples in the plurality of sequential samples.

7. The method as recited in Claim 1, further comprising:

calculating, in parallel, a third multiplication product of a second coefficient and a third sample and a fourth multiplication product of the second coefficient and a fourth sample;

wherein the third sample and the fourth sample are from the plurality of sequential samples;

wherein the third sample is an (n+1)th sample and the second sample is an (n+3)th sample in the plurality of sequential samples

8. The method as recited in Claim 1, further comprising:

calculating, in parallel a fifth multiplication product of a second coefficient and the first sample, and a sixth multiplication product of the second coefficient and the second sample generating a sixth product, and

accumulating in parallel, the fifth multiplication product with the first multiplication product and the sixth multiplication product with the second multiplication product.

9. The method as recited in Claim 5, wherein the first coefficient and second coefficient are filter coefficients.

10. The method as recited in Claim 1, wherein the calculating in parallel comprises executing a multiply accumulate single-instruction-multiple-data (SIMD) instruction.

11. A method comprising:

calculating a finite impulse response (FIR), wherein the calculating includes executing, in parallel, a first multiply accumulate operation of a first sample with a first coefficient and a second multiply accumulate operation of a second sample with the first coefficient;

wherein the first sample and the second sample are from a plurality of sequential samples;

wherein the first sample is an (n)th sample and the second sample is an (n+2)th sample in the plurality of sequential samples.

12. The method as recited in Claim 11, wherein the executing, in parallel, comprises:

selecting the first sample in a first location of an upper half of a first register and selecting the second sample in a corresponding location of a lower half of the first register;

selecting a first operand in a first location of an upper half of a second register and selecting a second operand in a corresponding location of a lower half of the second register, wherein the first operand and the second operand are each the first coefficient;

multiplying the first sample and the first operand and accumulating a first result in a lower half of a third register; and

multiplying the second sample and the second operand and accumulating a second result in an upper half of the third register.

13. The method as recited in Claim 12, further comprising saturating the first result and the second result.

14. The method as recited in Claim 12, wherein the first location and the corresponding location of the first register are one of the upper bits of each half of the first register and the lower bits of each half of the first register.

15. The method as recited in Claim 11, wherein the first coefficient is a filter coefficient.

16. The method as recited in Claim 11, wherein the calculating in parallel comprises executing a multiply accumulate single-instruction/multiple-data (SIMD) instruction.

17. An apparatus comprising:

a first plurality of multiplexers to select a first sample in a first location of an upper half of a first register and a second sample in a corresponding location of a lower half of the first register;

a second plurality of multiplexers to select a first operand in a first location of an upper half of a second register and a second operand in a corresponding location of a lower half of the second register, wherein the first operand and the second operand are each a first coefficient;

a first multiplier to multiply the first sample with the first operand; and

a second multiplier to multiply the second sample with the second operand;

wherein the first sample and the second sample are from a plurality of sequential samples;

wherein the first sample is an (n)th sample and the second sample is an (n+2)th sample in the plurality of sequential samples.

18. The apparatus as recited in Claim 14, further comprising:

a first accumulator to accumulate a first product of the first multiplier; and

a second accumulator to accumulate a second product of the second multiplier.

19. The apparatus as recited in Claim 14, where a first selection control for the first plurality of multiplexers and a second selection control for the second plurality of multiplexers is according to a first qualifier and a second qualifier specified in a single-instruction/multiple-data (SIMD) instruction.

20. The apparatus as recited in Claim 14, wherein the first coefficient is a filter coefficient.

21. An apparatus comprising:

a first plurality of multiplexers to select a first sample in a first location of an upper half of a first register and a second sample in a corresponding location of a lower half of the first register;

a second plurality of multiplexers to select a first operand in a first location of an upper half of a second register and a second operand in a corresponding location of a lower half of the second register, wherein the first operand and the second operand are each a first coefficient;

a first multiplier to multiply the first sample with the first operand; and

a second multiplier to multiply the second sample with the second operand;

wherein the first sample and the second sample are from a plurality of sequential samples;

wherein the first sample is an (n)th sample and the second sample is an (n+2)th sample in the plurality of sequential samples.

22. The apparatus as recited in Claim 21, the apparatus further comprising:

a first accumulator to accumulate a first product of the first multiplier; and

a second accumulator to accumulate a second product of the second multiplier.

23. The apparatus as recited in Claim 21, where a first selection control for the first plurality of multiplexers and a second selection control for the second plurality of multiplexers is according to a first qualifier and a second qualifier specified in a single-instruction/multiple-data (SIMD) instruction.

24. The apparatus as recited in Claim 21, wherein the first coefficient is a filter coefficient.

25. A data processing system comprising:

an addressable memory to store an instruction for a multiply-accumulate operation;

a processing core coupled to the addressable memory, the processor core comprising:

an execution core to access the instruction;

a first source register to store a plurality of sequential samples;

a second source register to store a plurality of coefficients; and

a destination register to store a plurality of results;

a wireless interface to receive data; and

an I/O system and decoder to provide the plurality of samples to the first source register from the data;

wherein the execution core comprises:

a first plurality of multiplexers to select a first sample in a first location of an upper half of a first register and a second sample in a corresponding location of a lower half of the first register;

a second plurality of multiplexers to select a first operand in a first location of an upper half of a second register and a second operand in a corresponding location of a lower half of the second register, wherein the first operand and the second operand are each a first coefficient;

a first multiplier to multiply the first sample with the first operand; and

a second multiplier to multiply the second sample with the second operand;

wherein the first sample is an (n)th sample and the second sample is an (n+2)th sample in the plurality of sequential samples.

26. The data processing system as recited in Claim 25, the execution unit further comprising:

a first accumulator to accumulate a first product of the first multiplier; and

a second accumulator to accumulate a second product of the second multiplier.

27. The data processing system as recited in Claim 25, where a first selection control for the first plurality of multiplexers and a second selection control for the second plurality of multiplexers is according to a first qualifier and a second qualifier specified in a single-instruction/multiple-data (SIMD) instruction.

28. The data processing system as recited in Claim 25, wherein the first coefficient is a filter coefficient.

29. An article comprising a storage medium having instructions stored thereon, the instructions operable to:

calculate, in parallel, a first multiplication product of a first coefficient and a first sample, and a second multiplication product of the first coefficient and a second sample;

wherein the first sample and the second sample are from a plurality of sequential samples;

wherein the first sample is an (n)th sample and the second sample is an (n+2)th sample in the plurality of sequential samples.

30. The article as recited in Claim 29, wherein the first sample and second sample are odd samples in the plurality of sequential samples.

31. The article as recited in Claim 29, wherein the first sample and second sample are even samples in the plurality of sequential samples.

32. The article as recited in Claim 29, the instructions further operable to:

calculate, in parallel, a third multiplication product of a second coefficient and a third sample and a fourth multiplication product of the second coefficient and a fourth sample;

wherein the third sample and fourth sample are from the plurality of sequential samples;

wherein the third sample is an (n+1)th sample and the second sample is an (n+3)th sample in the plurality of sequential samples

33. The article as recited in Claim 29, the instructions further operable to:

calculate, in parallel a fifth multiplication product of a second coefficient and the first sample, and a sixth multiplication product of the second coefficient and the second sample generating a sixth product, and

accumulate in parallel, the fifth multiplication product with the first multiplication product and the sixth multiplication product with the second multiplication product.

34. The article as recited in Claim 33, wherein the first coefficient and second coefficient are filter coefficients.

35. The article as recited in Claim 29, wherein to calculate in parallel comprises to execute a multiply accumulate single-instruction-multiple-data (SIMD) instruction.